Abstract of the Disclosure

NROM EEPROM memory devices and arrays are described that facilitate the use of vertical NROM memory cells and select gates in NOR or NAND high density memory architectures. Memory embodiments of the present invention utilize vertical select gates and NROM memory cells to form NOR and NAND NROM architecture memory cell strings, segments, and arrays. These NROM memory cell architectures allow for improved high density memory devices or arrays with integral select gates that can take advantage of the feature sizes semiconductor fabrication processes are generally capable of and yet do not suffer from charge separation issues in typical multi-bit NROM cells. The memory cell architectures also allow for mitigation of disturb and overerasure issues by placing the NROM memory cells behind select gates that isolate the memory cells from their associated bit/data lines and/or source lines.